a command stream controller to manipulate motion compensated video data;

a write address generator coupled to the command stream controller;

a memory coupled to the command stream controller and to the write address generator, the memory to store pixel data in a first order determined by the write address generator;

processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame; and

a read address generator coupled to the processing circuitry and to the memory, the read address generator to cause the memory to output pixel data in a second order, wherein the second order comprises a sub-block-by-sub-block in row major order.

30. (New) The circuit of claim 29, wherein the processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame comprises processing circuitry to perform motion compensation operations and texture mapping operations utilizing common circuitry.

31. (New) The circuit of claim 29, wherein the first order corresponds to an output sequence of an inverse discrete cosine transform operation.

32. (New) The circuit of claim 29, wherein the first order is block by block in row major order.

33. (New) The circuit of claim 29, wherein the processing circuitry comprises a setup engine that determines a bounding box for pixels manipulated by the instruction, wherein the bounding box contains all edges of a macroblock.

34. (New) The circuit of claim 29, wherein the processing circuitry comprises a windower having a first mode wherein pixels inside a triangle within a bounding box are processed, and a second mode wherein all pixels within the bounding box are processed.

35. (New) The circuit of claim 29, wherein the circuit is pipelined.

36. (New) An apparatus comprising:

a command stream controller to manipulate motion compensation video data;

a memory coupled to the command stream controller, the memory to store pixel data related to a macroblock in a first order, the first order is based on output from an Inverse Discrete Cosine Transform (IDCT) operation;

a read address generator coupled to the memory, the read address generator to cause the memory to output the pixel data related to a macroblock in a second order, the read address generator to cause the memory to output pixel data in sub-block-by-sub-block in row major order; and

a processing unit coupled to the read address generator and to the command stream controller, the processing unit to perform motion compensation operations and texture mapping operations utilizing common circuitry.

37. (New) The apparatus of claim 36, wherein the memory to store pixel data related to a macroblock in a first order comprises the memory to store pixel data related to a macroblock block by block in row major order.

38. (New) The apparatus of claim 36, wherein the processing unit further comprises:

a memory to store reference pixels;

a mapping address generator to provide read addresses for the reference pixels;

a bilinear filter coupled to the memory, the bilinear filter to access the reference pixels from the memory and to filter the reference pixels; and

a first-in-first-out (FIFO) buffer coupling the mapping address generator to the bilinear filter, the buffer to maintain sequence of the read addresses from the mapping address generator to the bilinear filter.

39. (New) The apparatus of claim 36, further comprising the read address generator coupled to a write address generator, the write address generator to generate synch points and the read address generator to receive the synch points to prevent the read address generator from overwriting valid data in the memory.

40. (New) The apparatus of claim 36, wherein the apparatus is pipelined.

41. (New) A method comprising:

storing pixel data in a memory in a first order based on output from an Inverse Discrete Cosine Transform (IDCT) operation;

receiving a command to generate a reconstructed video frame; and

reading the pixel data out of the memory in a second order, wherein the second order comprises reading the pixel data sub-block-by-sub-block in row major order.

42. (New) The method of claim 41, wherein storing pixel data in a memory in a first order based on output from an Inverse Discrete Cosine Transform (IDCT) operation comprises storing pixel data block by block in row major order.

43. (New) The method of claim 41, further comprising determining a bounding box for pixels manipulated by the instruction, wherein the bounding box contains all edges of a macroblock.

44. (New) The method of claim 43, further comprising processing the pixel data in triangular regions, wherein in a first mode pixels inside a triangle within a bounding box are processed, and in a second mode all pixels within the bounding box are processed.

45. (New) A method of motion compensation of digital video data, the method comprising:

receiving a motion compensation command having associated correction data related to a macroblock;

storing the correction data in a memory block by block in row major order;

performing frame prediction operations in response to the motion compensation command;

reading the correction data from the memory sub-block by sub-block in row major order; and

combining the correction data with results from the frame prediction operations to generate an output video frame.

46. (New) The method of claim 45, wherein performing frame prediction operations further comprises:

generating a bounding box containing the macroblock; and

iterating the bounding the bounding box;

fetching reference pixels;

filtering the reference pixels;

averaging the filtered reference pixels, if necessary; and

adding correction data to the reference pixels.

47. (New) The method of claim 46, further comprising performing texturing operations for the macroblock.

48. (New) An article of manufacture comprising:

an electronically accessible medium providing instructions that, when executed by one or more processors, cause the one or more processors to

receive a motion compensation command having associated correction data related to a macroblock;

storing the correction data in a memory block by block in row major order;

perform frame prediction operations in response to the motion compensation command;

read the correction data from the memory sub-block by sub-block in row major order; and

combine the correction data with results from the frame prediction operations to generate an output video frame.

49. (New) The article of manufacture of claim 48, wherein the electronically accessible medium further comprises instructions that, when executed by one or more processors, cause the one or more processors to

generate a bounding box containing the macroblock; and

iterate the bounding the bounding box;

fetch reference pixels;

filter the reference pixels;

average the filtered reference pixels, if necessary; and

add correction data to the reference pixels.

50. (New) The article of manufacture of claim 49, wherein the electronically accessible medium further comprises instructions that, when executed by one or more processors, cause the one or more processors to perform texturing operations for the macroblock.